

[illegible]

A cross-sectional view of a semiconductor device. A substrate 1 is shown at the bottom, with a layer 2 on top of it. A central gate structure 13 is formed on the substrate, consisting of a gate dielectric layer 3 and a gate electrode 5. The gate electrode 5 is connected to a terminal 6. The gate structure 13 is flanked by two side regions 8. The side regions 8 are separated from the gate structure 13 by a gap 14. The side regions 8 are connected to a terminal 4. The side regions 8 are also connected to a terminal 15. The side regions 8 are separated from the gate structure 13 by a gap 14. The side regions 8 are connected to a terminal 4. The side regions 8 are also connected to a terminal 15.

Fig. 2A

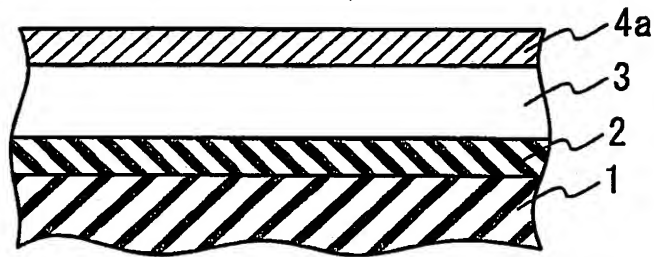


Fig. 2B

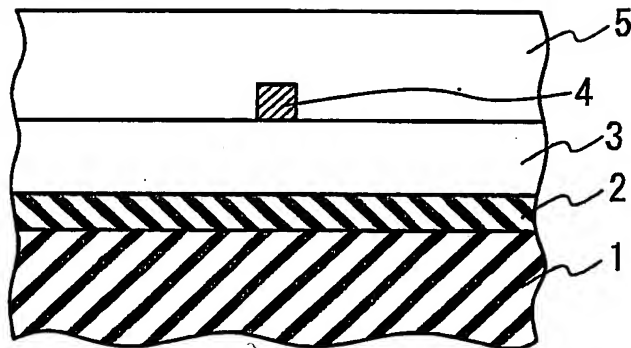


Fig. 2C

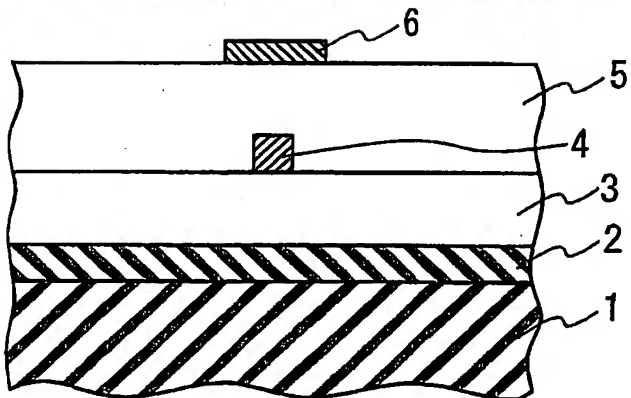


Fig. 2D

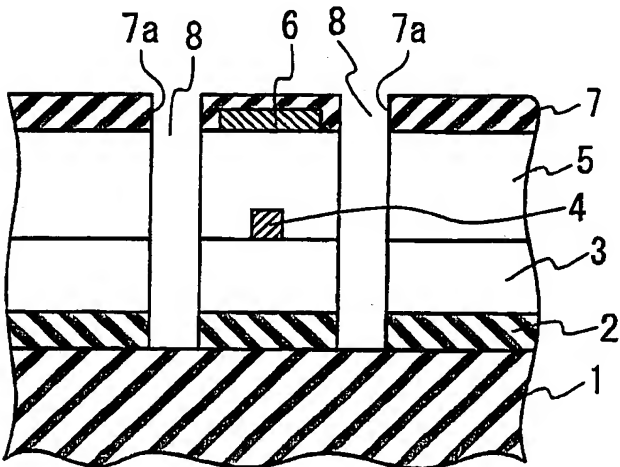


Fig. 3A

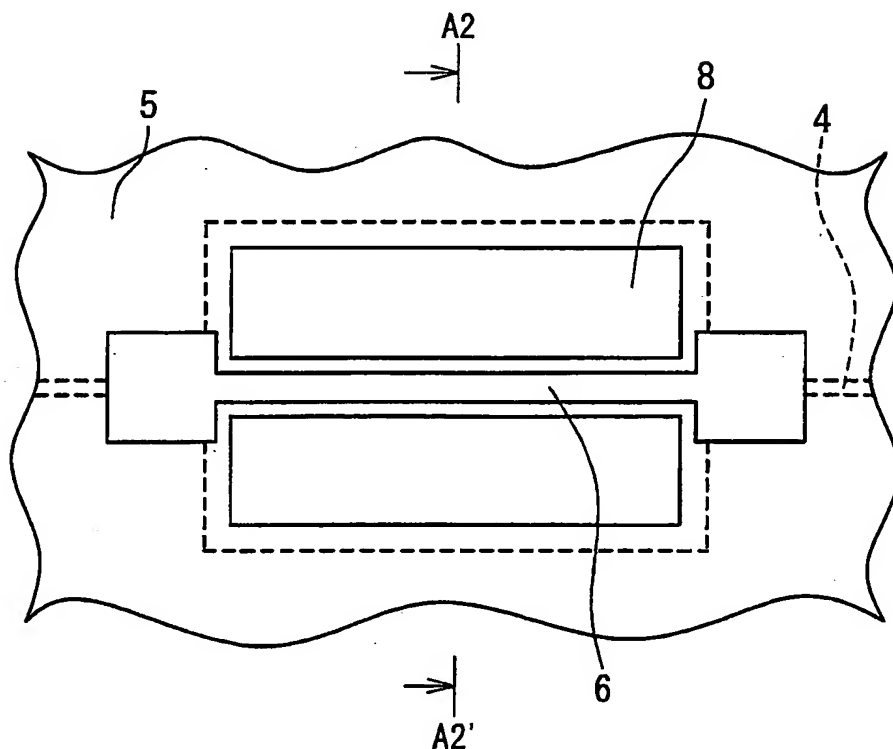


Fig. 3B

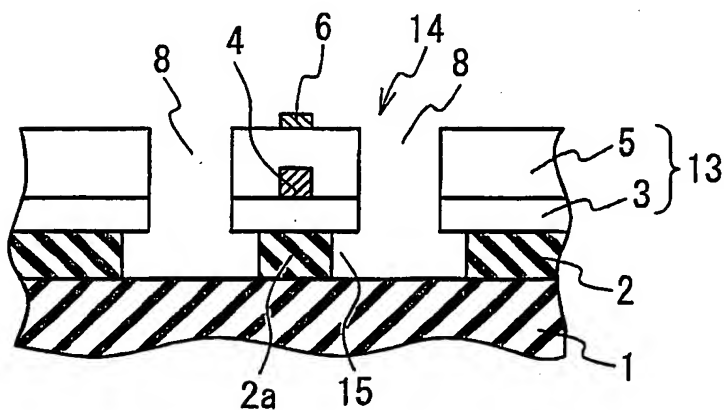


Fig. 4A

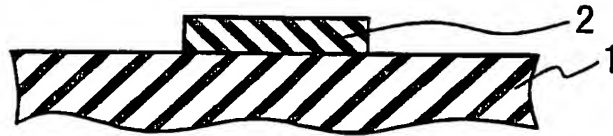


Fig. 4B

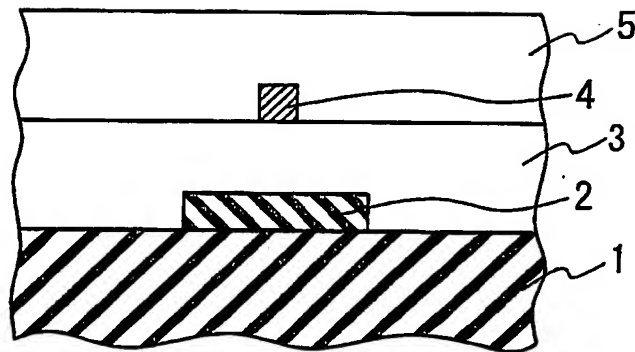


Fig. 4C

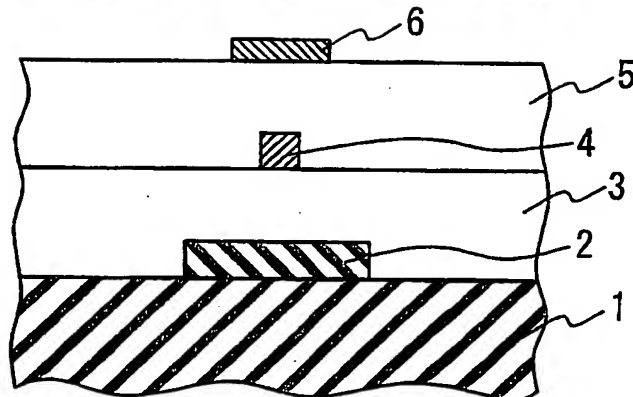


Fig. 4D

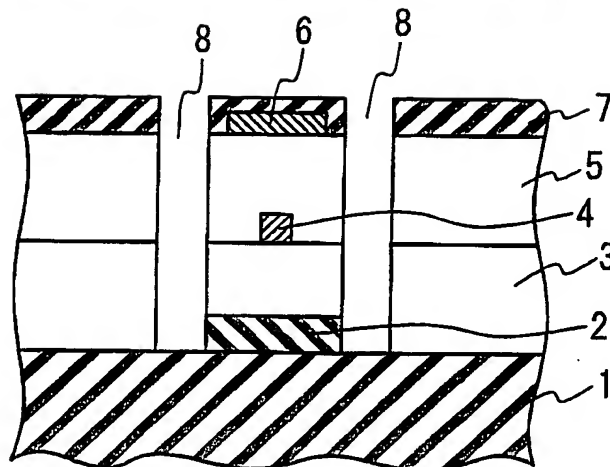


Fig. 5A

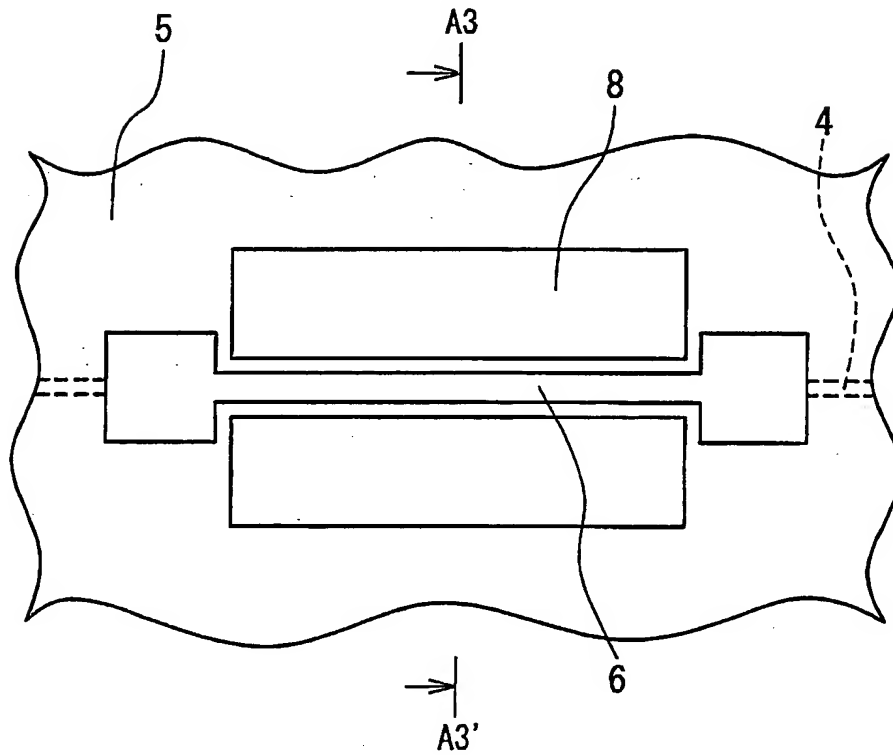


Fig. 5B

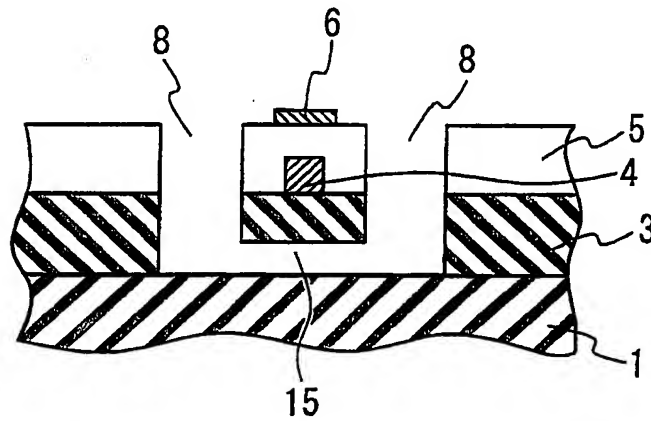


Fig. 6A

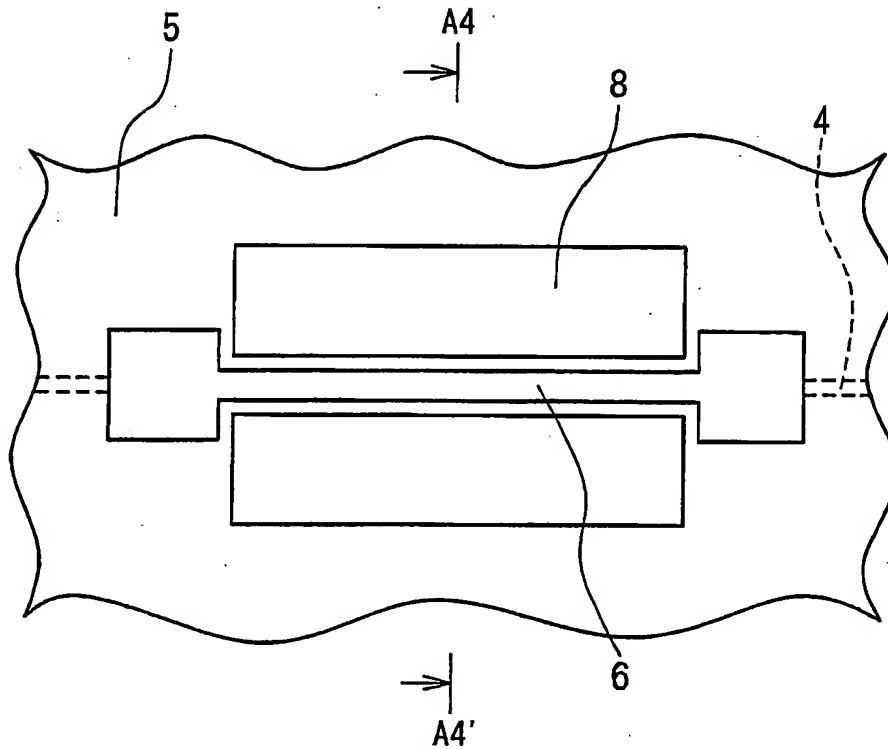


Fig. 6B

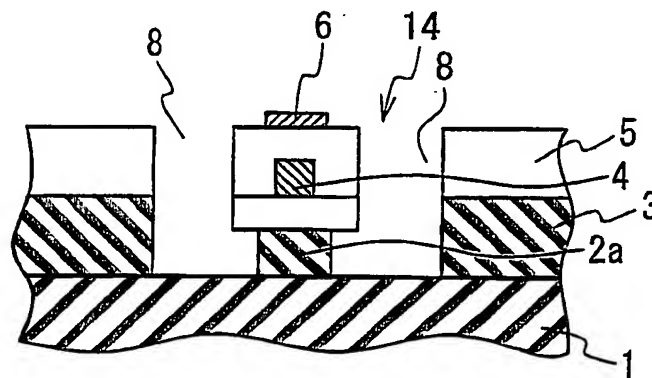


Fig. 7A

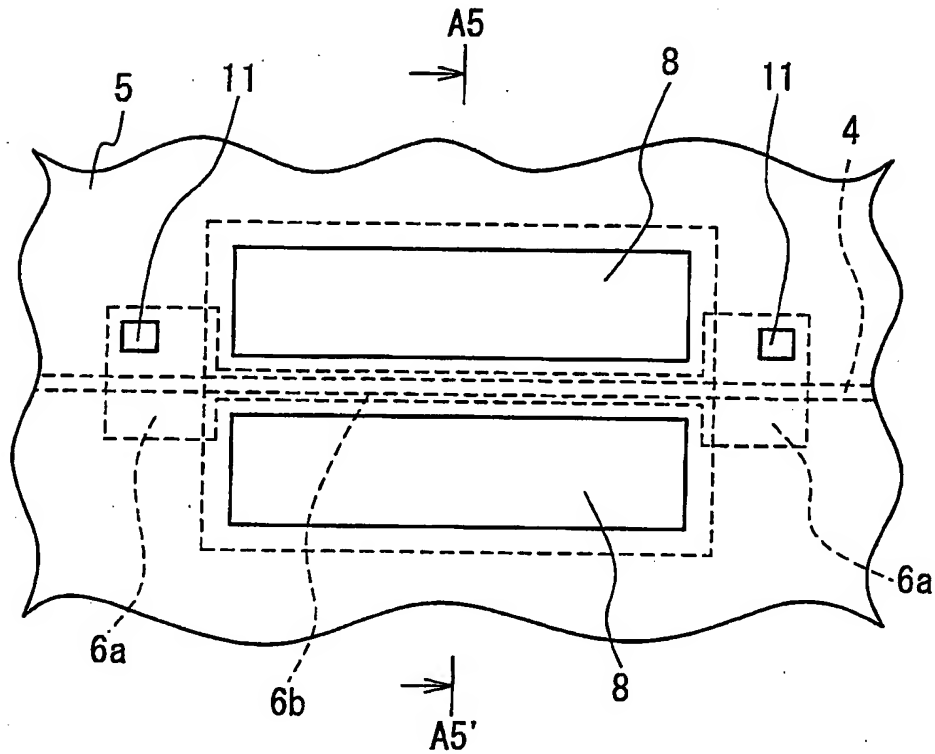


Fig. 7B

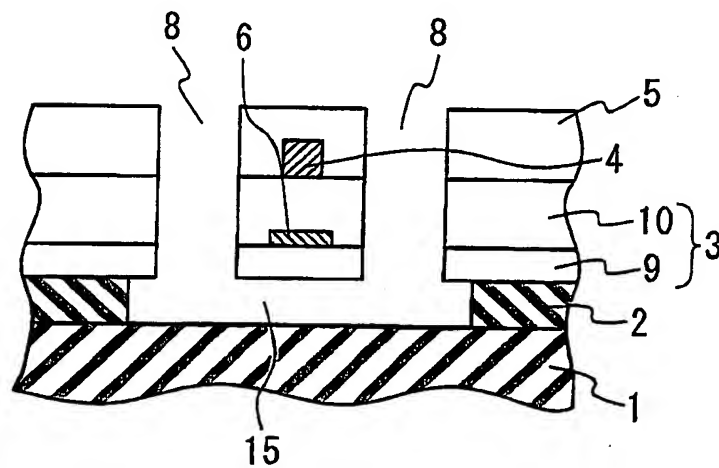


Fig. 8A

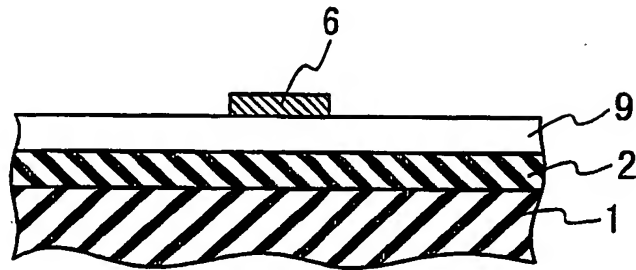


Fig. 8B

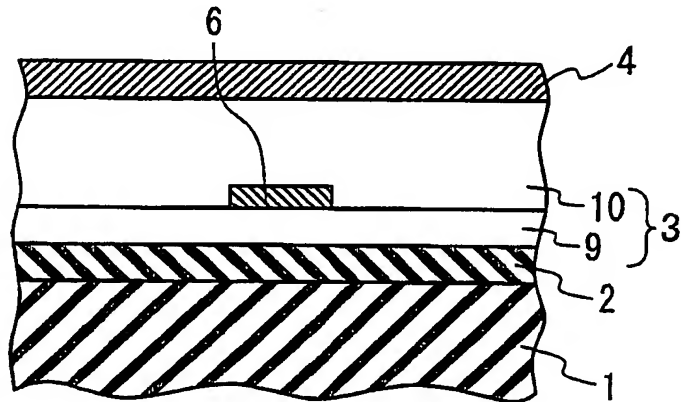


Fig. 8C

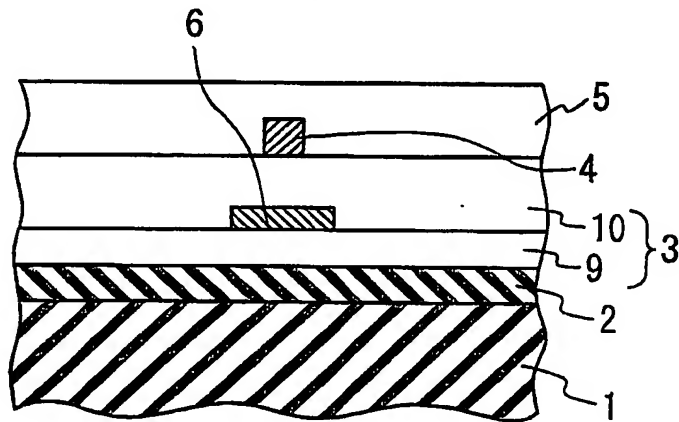


Fig. 8D

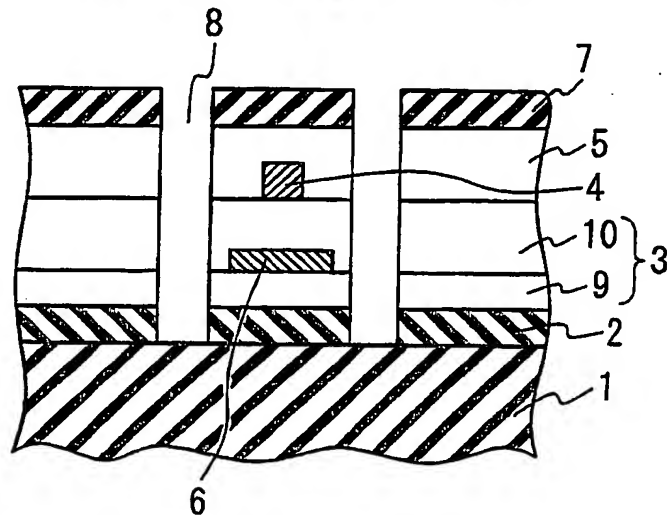




Fig. 9A

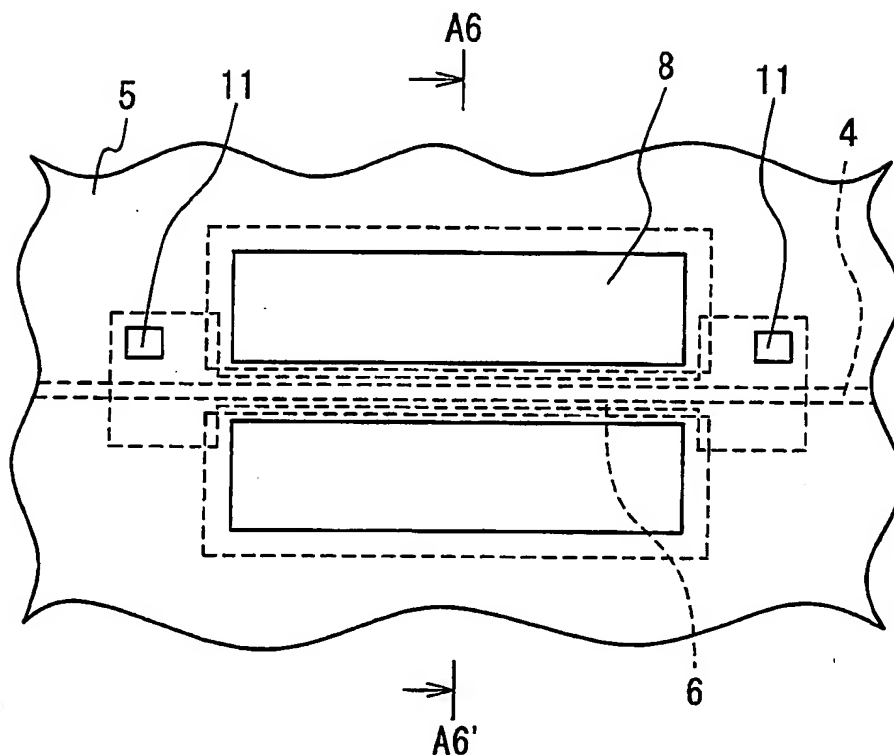


Fig. 9B

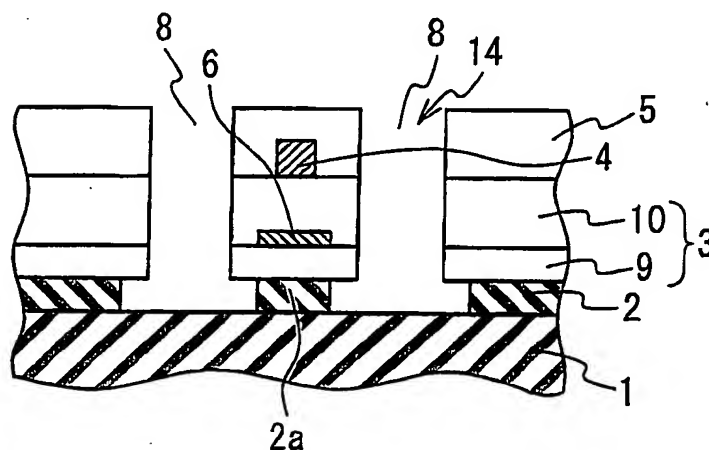


Fig. 10A

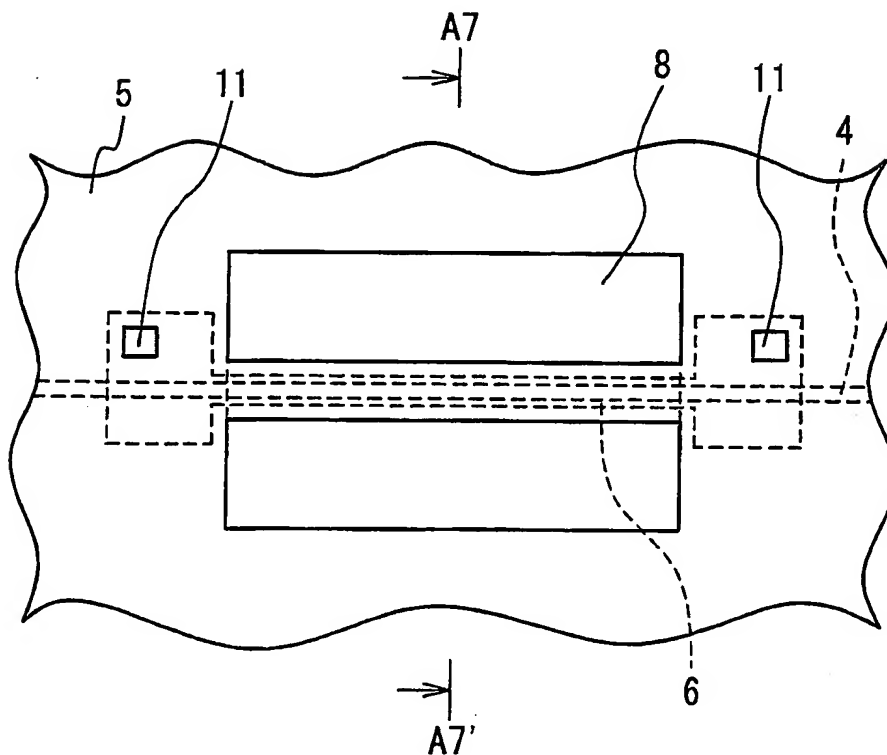


Fig. 10B

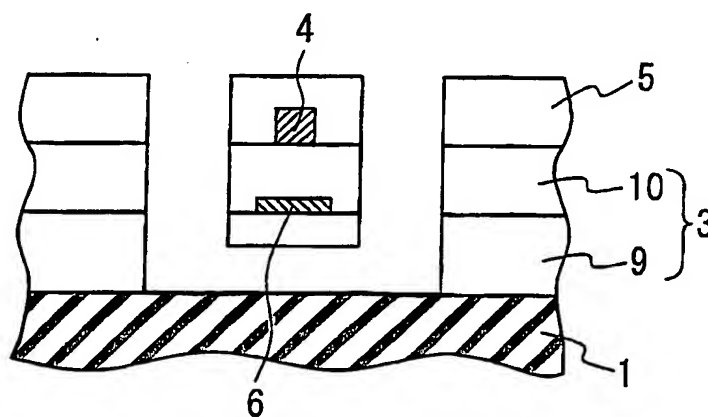


Fig. 11A

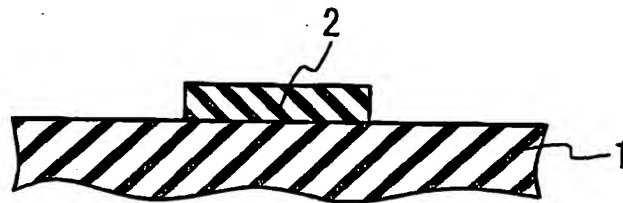


Fig. 11B

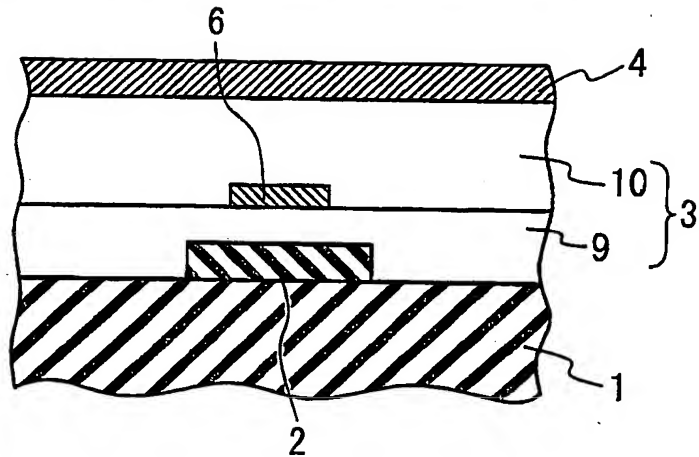


Fig. 11C

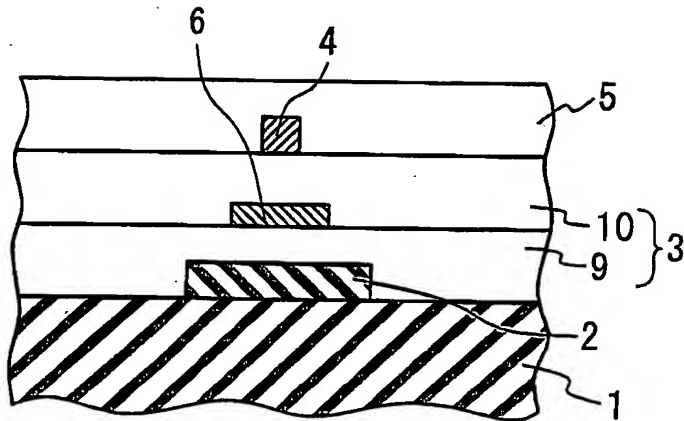


Fig. 11D

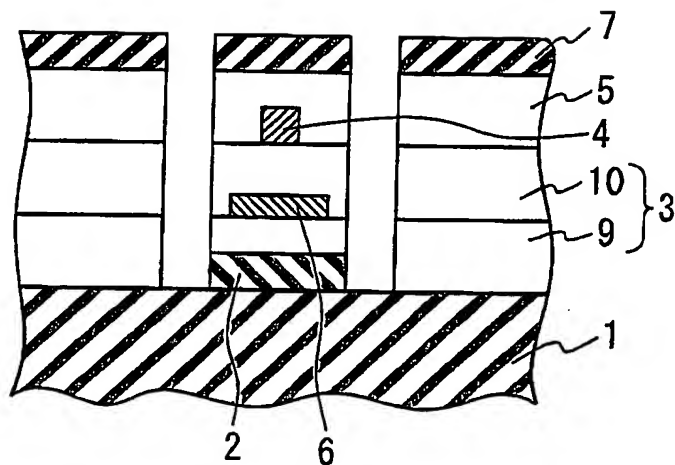


Fig. 12A

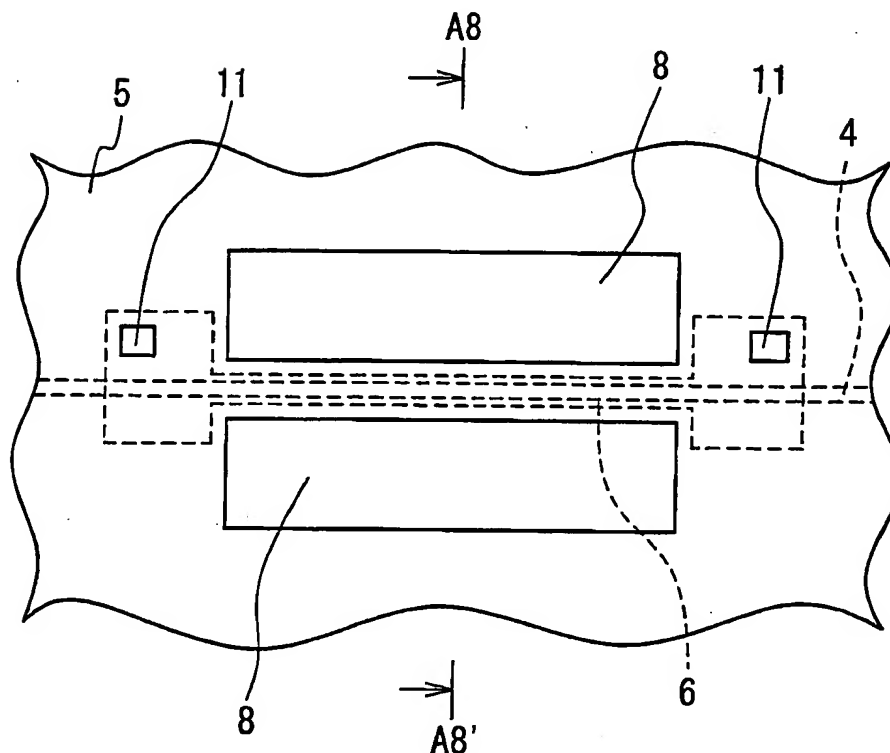


Fig. 12B

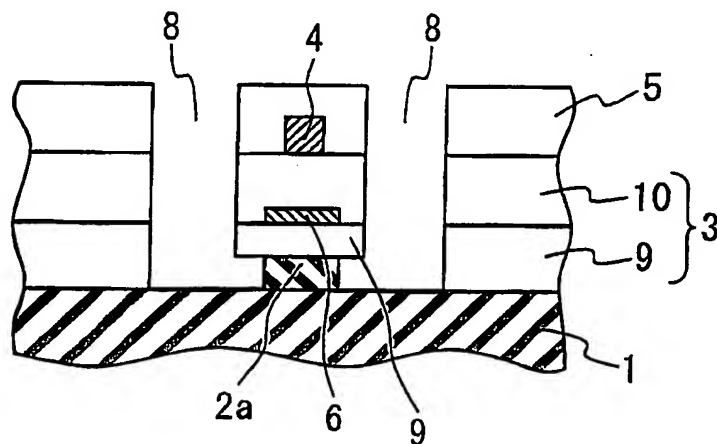


Fig. 13A

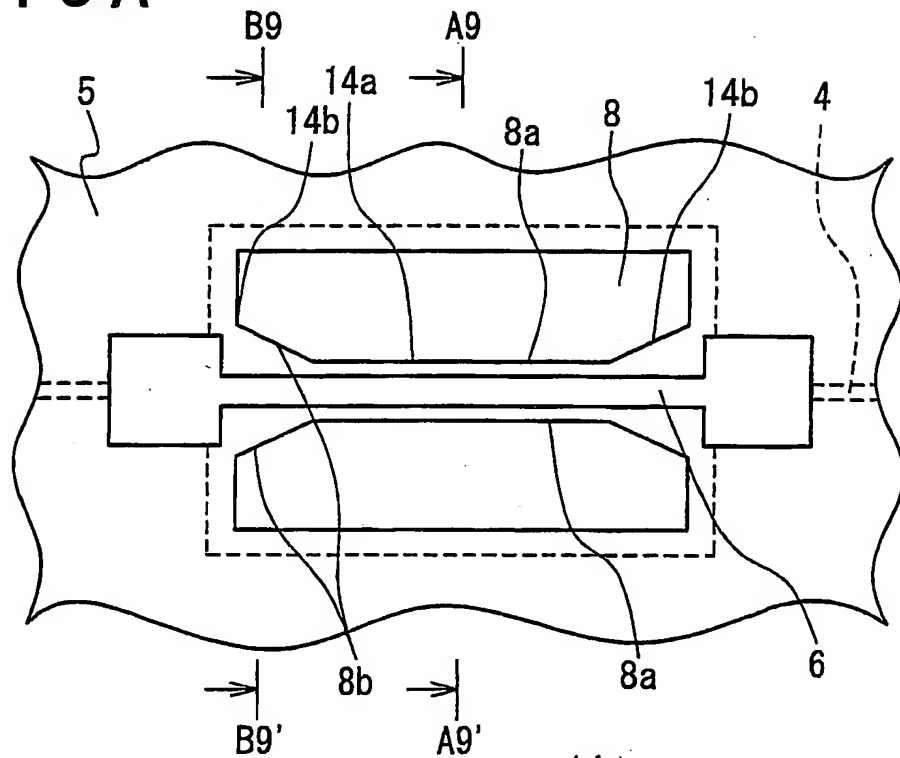


Fig. 13B

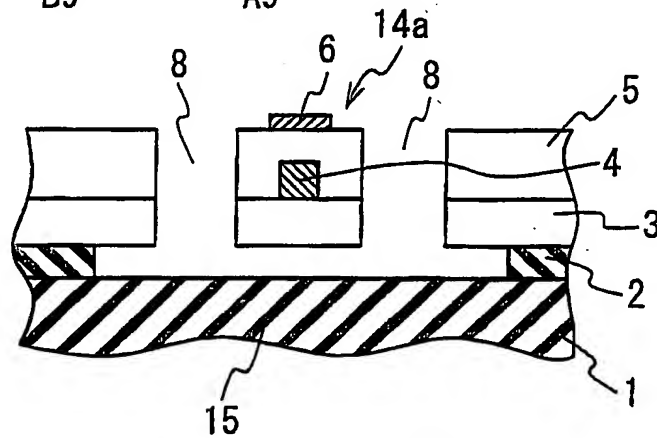


Fig. 13C

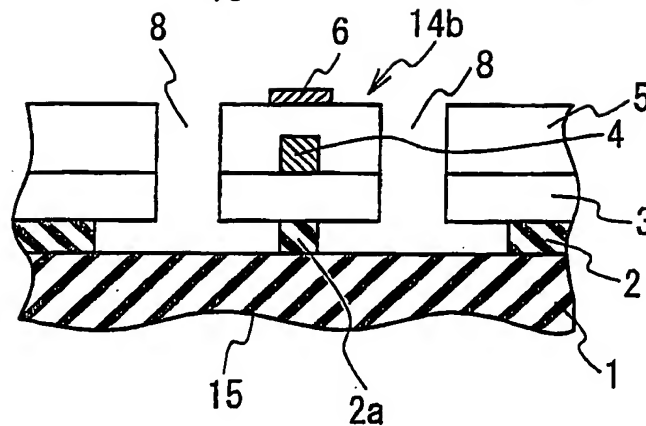


Fig. 14A

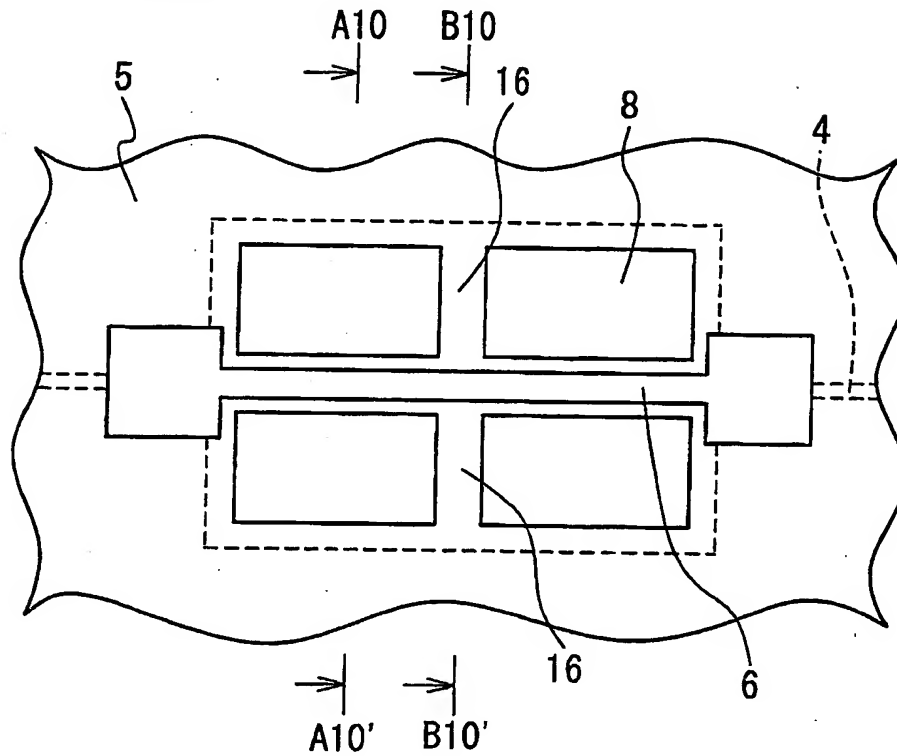


Fig. 14B

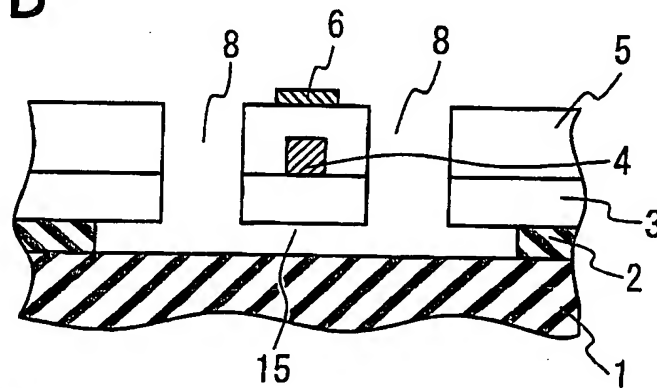


Fig. 14C

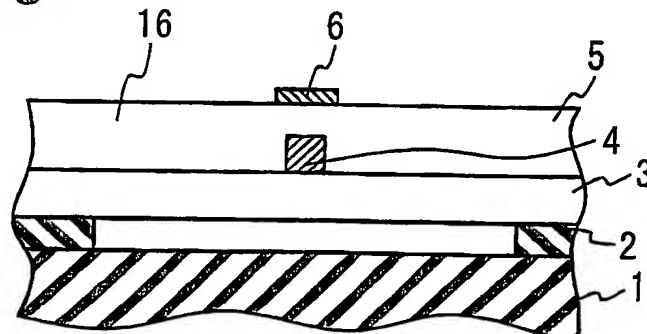


Fig. 15A

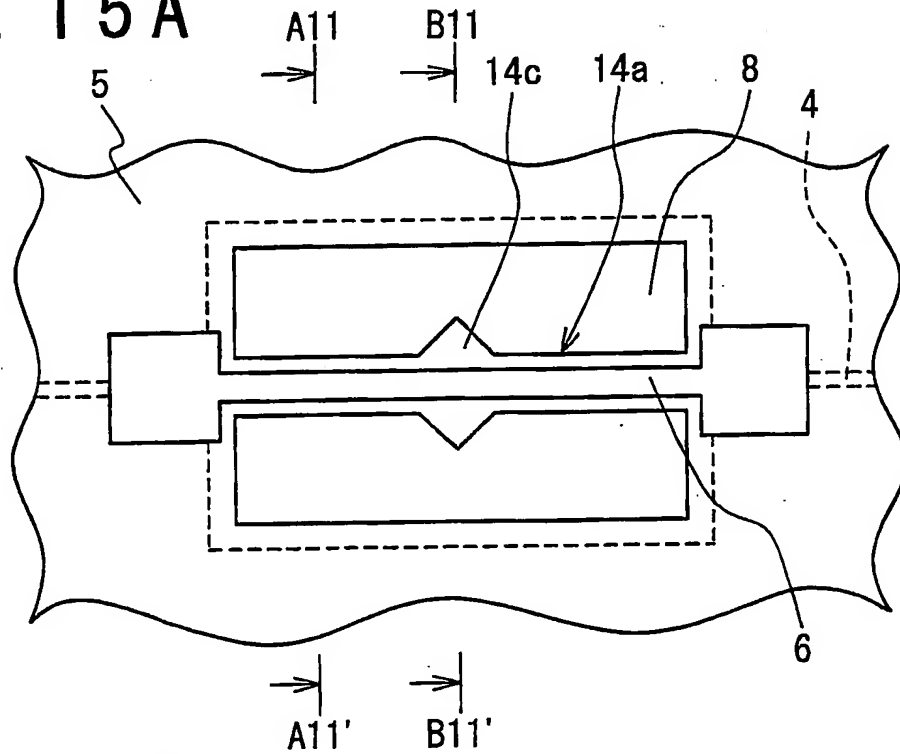


Fig. 15B

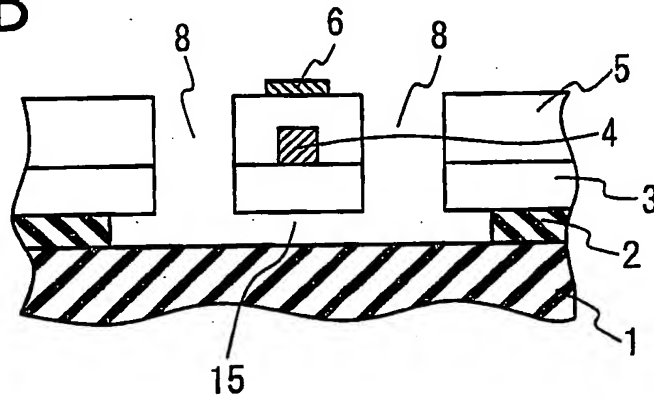


Fig. 15C

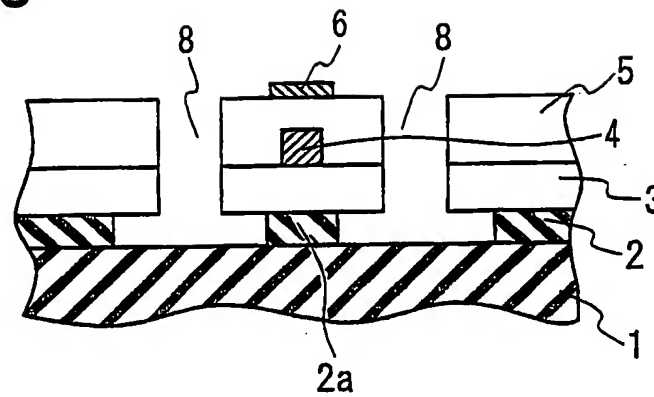


Fig. 16A

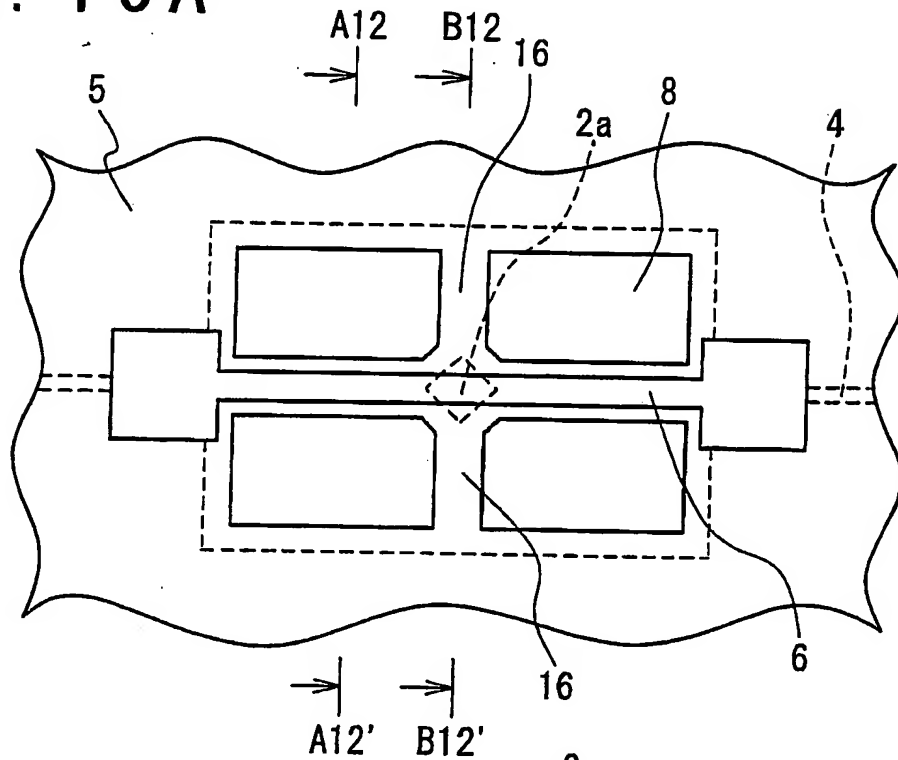


Fig. 16B

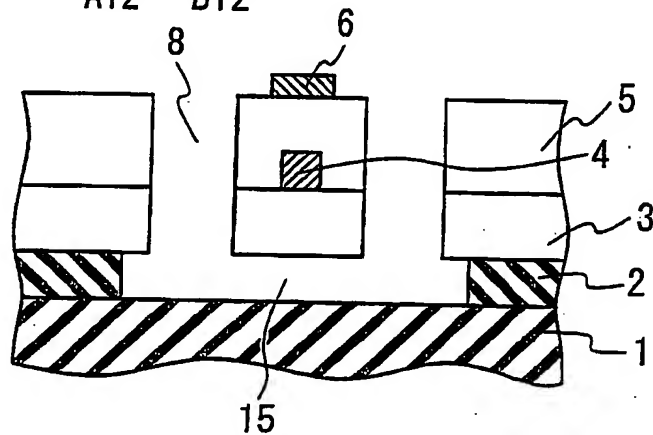


Fig. 16C

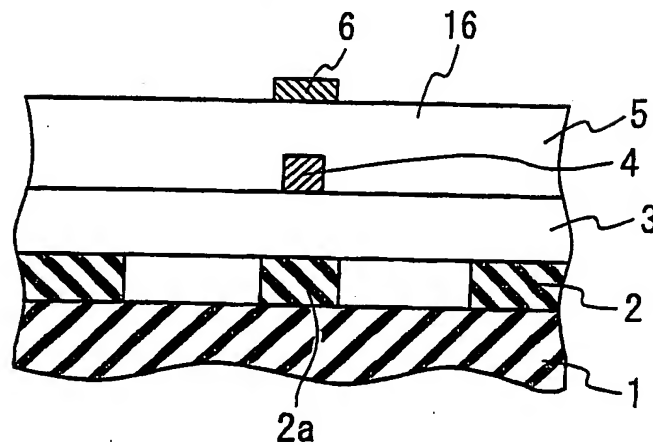




Fig. 17A

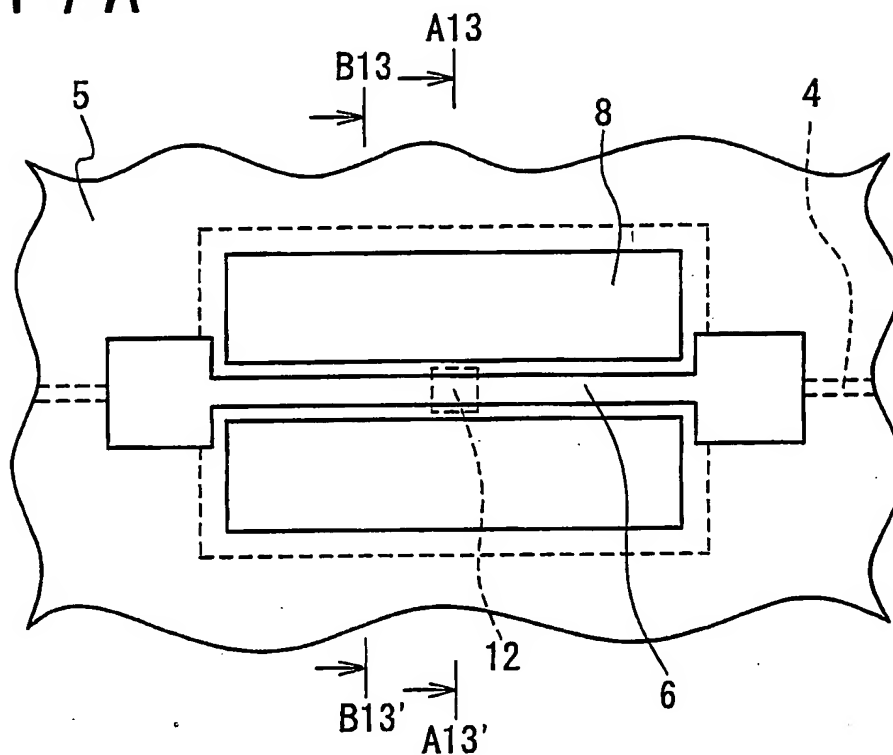


Fig. 17B

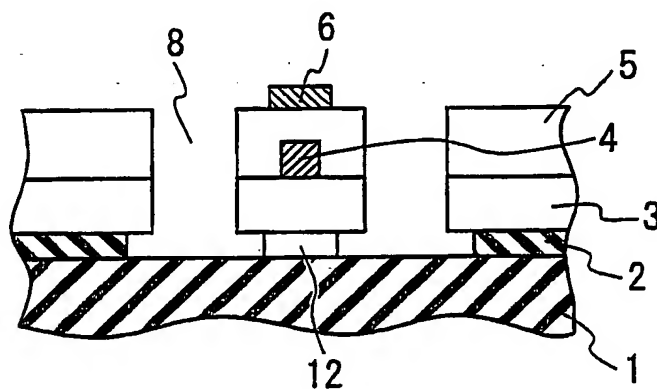


Fig. 17C

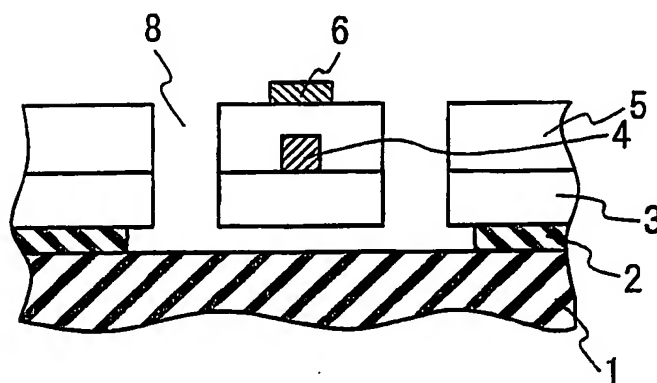


Fig. 18A

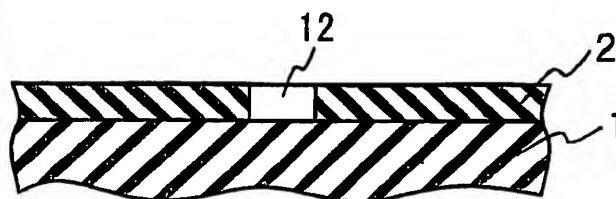


Fig. 18B

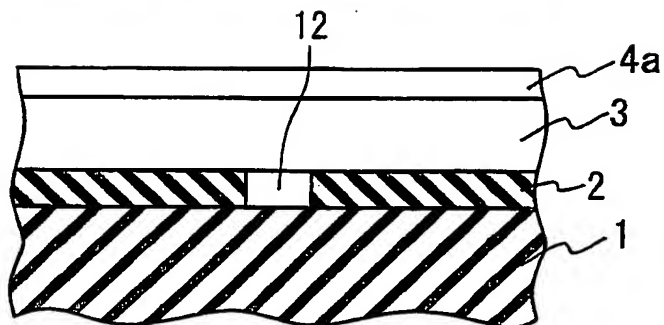


Fig. 18C

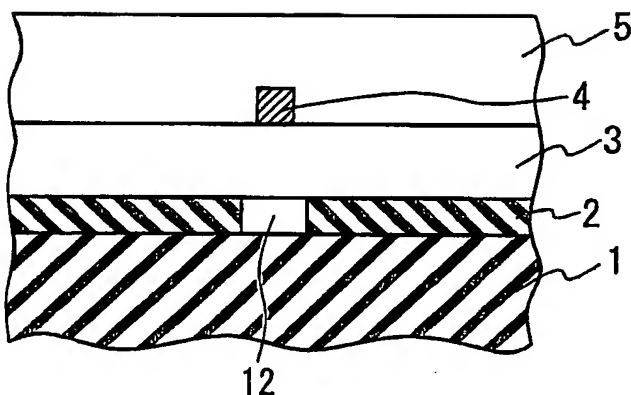


Fig. 18D

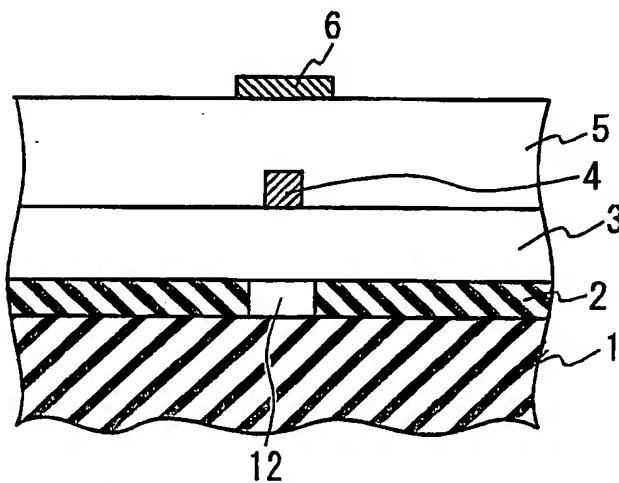


Fig. 19

